The analog under-ware of quantum networks: simulation, abstraction and protocol design

Advanced communication networks incorporate heterogeneous hardware components and serve a diverse range of application needs at once. The smart specification (by designers/engineers) and rigorous implementation (by device makers and programmers) of protocol "stacks" play crucial roles in enabling this miracle of robust performance. Indeed, in the modern era we rely ubiquitously on principles of modularity and abstraction to facilitate hierarchical engineering of complex systems.

Given the advanced state of conventional computing hardware, however, it is not often that we give much thought to the very lowest levels of protocol stacks, in which clocked digital informational structures are grafted onto the analog continuous-time physical dynamics of their underlying hardware. Considering the panoply of basic physical mechanisms used today for storing, transmitting and processing information (*e.g.*, magnetic recording, optical readout, surface acoustic wave filtering, electromagnetic wave propagation, …) that can effortlessly be harnessed to retrieve internet search results on a mobile phone, it seems clear that these analog foundation layers have been very well conceived and engineered in the classical setting.

For the foreseeable future, prototype *quantum* networks for secure communication and distributed sensing are likely to be characterized by extreme hardware diversity and will need to be configured to support a wide range of algorithms. To date, however, very little research has focused on the formulation of abstraction principles or notions of modularity that can serve as design interfaces between the raw analog physics of real devices and the computer scientist's world of qubits and discretized transformations. What essential aspects of a hardware device's behavior should a "machine code" programmer be able to take for granted, which enable him/her to develop powerful algorithms yet can reasonably well be guaranteed by the makers of devices based on arbitrary physical principles? Maximum input-output latency? Residual entanglement between output symbols and the device's internal state (which could lead to correlated errors)? Sensitivity to timing errors in the presentation of input signals (*e.g.*, propagation time delays)?

In addition to facilitating standardization, low-level protocols can play a crucial role in enabling confident simulation of complex network algorithms and architectures by "hiding" some internal details of individual components from network-level dynamics. To cite a well-known example from classical electrical engineering, we all know that high-performance operation amplifiers may comprise numerous discrete internal components with complex nonlinear dynamics; on the other hand, we can perform basic analysis of op-amp circuits rather straightforwardly if we can count on the fact that the op-amps behave in the modular way they are supposed to, with infinite input impedance and zero output impedance, and so forth. We are far from understanding in general how to design quantum network components in ways that admit such model-reducing abstractions, however we know some examples of rigorous methods based on singular perturbation in models based on quantum stochastic differential equations [Bout08,Kerc10]. The latter work characterizes a sort of "small-volume" limit in nanophotonic implementations of cavity QED, which is natural to consider for engineering reasons (as smaller resonators achieve stronger light-matter coupling), in which the *ab initio* dynamic model of a nanophotonic device can be replaced by a quantum scattering model with no internal state. This approximation becomes accurate when we consider the dynamics of the overall network/circuit in which the component is embedded on timescales long compared to the ring-down time of an individual resonator; this ring-down time tends to zero in the small volume limit.

We seem to be at a crucial moment in the development of quantum information science, at which we have an opportunity to develop and promote smart abstraction principles at the next-to-hardware level in quantum engineering. We have a wide range of hardware platforms to consider and a broad (if not comprehensive) view of potential quantum network applications. Good protocols at this level would facilitate "plug and play" interoperability of near-term research platforms and would provide useful checklists of specifications that new physical components would need to meet, as well as limitations on what network architects and algorithm designers should be able to assume in terms of the behavior of underlying hardware. For scaling analyses and extrapolations of potential full-scale performance, they could also enable meaningful simulation of low-dimensional models of large quantum networks. While this type of research may not directly lead to the discovery of new high-impact network applications, it will be crucial for ensuring we have the foundations to implement such applications robustly in the near future.

References

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